



# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Topside Metal:**  
**Backside:**  
**Backside Potential:**  
**Mask Ref:**  
**Bond Pads (Mils):**

**APPROVED BY:**  
**MFG: M.S.**

**DIE SIZE (Mils): 60 x 60**  
**THICKNESS:**

**DATE: 3/16/00**  
**P/N: CHP5KE13CA**

DG 10.1.2  
Rev A 3-4-99